AMENDMENTS TO THE CLAIMS

1-7. (Canceled)

8. (Currently amended) An integrated circuit device comprising:

at least one functional module which has a plurality of flip-flops forming a scan chain, wherein the functional module performs a saving operation by outputting data in the flip-flops by a shift operation using the scan chain synchronized with a saving clock signal, and performs a restoring operation by restoring, to the flip-flops, the saved data by a shift operation using scan the chain synchronized with a restoration clock signal;

a power supply control unit which selects one of the functional modules, and controls stop and resumption of power supply to the selected functional module;

a clock signal generator which generates a saving clock signal and restoration clock signal for the functional module selected by the power supply control unit;

a scan controller which, in the saving operation or restoring operation, sets the functional module selected by the power supply control unit to a scan test mode, and selects the saving clock signal or restoration clock signal generated by the clock signal generator as a clock signal to be supplied for the shift operation using the scan chain;

a ~~save data storage unit~~ shift register connected to the scan chain, [[which]] wherein the shift register stores the save data output from the functional module selected by the power supply control unit by the shift operation using the scan chain synchronized with the saving clock signal; and

an error checking and correction unit which performs error checking and correction for the save data stored in the ~~save data storage unit~~ shift register when the save data is to be restored

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to the flip-flops of the functional module by the shift operation using the scan chain synchronized with the restoration clock signal.

9. (Currently amended) A device according to claim 8, wherein the clock signal generator generates a clock signal for use in periodic error checking and correction performed in the ~~save data storage unit~~ shift register.

10. (Currently amended) [[A]] The device according to claim 8, wherein the error checking and correction unit comprises:

an encoder which generates an error correction code from the save data, and writes the error correction code in the ~~save data storage unit~~ shift register; and

a decoder which reads out the stored save data and the corresponding error correction code from the ~~save data storage unit~~ shift register, and decodes the save data.

11. (Currently amended) [[A]] The device according to claim 8, wherein the error checking and correction unit periodically performs error checking and correction for the save data stored in the ~~save data storage unit~~ shift register.

12. (Currently amended) [[A]] The device according to claim 8, wherein

the ~~save data storage unit~~ shift register stores a plurality of copies of the save data, and

the error checking and correction unit performs error checking and correction by a majority operation using said plurality of copied data stored in the ~~save data storage unit~~ shift register.

13. (Currently amended) [[A]] The device according to claim 8, wherein the ~~save data storage unit~~ shift register is storage means for a built-in self-test circuit.

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14. (Currently amended) [[A]] The device according to claim 8, which further comprises:

a compressor which compresses the save data stored in the ~~save data storage unit~~ shift register; and

an expander which expands the save data compressed by the compressor when the save data is to be restored to the functional module.

15. (Canceled)

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